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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,174	06/30/2003	Peter J Jenkins	BUR920030012US1	1173

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EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,174	JENKINS ET AL.	
	Examiner	Art Unit	
	Sun J Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,14-16 and 20* is/are rejected.

7)☒ Claim(s) *4-6,11-13 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/604,174 filed on 06/30/2003. Claims 1 – 20 remain pending in the application.

Specification Objections

2. The specification is objected to because of following informalities:

Before Paragraph 0001, delete —**Description**—.

Before Paragraph 0001, change "BACKGROUND OF INVENTION" to —**BACKGROUND OF THE INVENTION**—.

Paragraph 0003, change "Related Art" to —**Description of Related Art**—.

Paragraph 0008, line 1, after "which" insert —**ones**—.

Paragraph 0008, line 2, change "take" to —**taken**—.

Paragraph 0009, line 3, after "which" insert —**one**—.

Before Paragraph 0010, change 'SUMMARY OF INVENTION" to —**SUMMARY OF THE INVENTION**—.

After Paragraph 0018, include a short description for Fig. 4.

Before Paragraph 0019, change "DETAILED DESCRIPTION" to —**DETAILED DESCRIPTION OF THE INVENTION**—.

Paragraph 0023, line 2, after "which" insert —**one**—.

Paragraph 0023, line 3, after "which" insert —**one**—.

Appropriate correction is required.

Drawing Objections

3. Drawings listed below are objected to because of following informalities:

Fig. 1 should be labeled as a —**(PRIOR ART)**—.

Fig. 2 should be labeled as a —**(PRIOR ART)**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 – 3, 8 – 10 and 14 – 16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,702,868 to *Kellam et al.* in view of IEEE paper entitled "*Package Clock Distribution Design Optimization for High-Speed and Low-Power VLSIs*" to *Zhu et al.*

6. As to Claim 1, *Kellam et al.* teach the following subject matter:

- *Conductive wiring patterns* of an *ASIC* (i.e., *Application Specific Integrated Circuit*) – [col. 2, line 25 – 26];
- ***Place*** *functional blocks* and ***route*** *the interconnecting wirings defining the overall functionality* of the ASIC – [col. 2, line 40 – 41]; Notice that (1) there are a plurality of intèrconnecting wirings between functional blocks of the ASIC, (2) the *interconnecting wirings* are *route paths* between the *functional blocks* of the ASIC, (3) the *route paths* (interconnecting wirings) are routed between appropriate terminals in order to define the *overall functionality* of the ASIC.

Kellam et al. do not teach a method of scanning the route path for transmission line replacement candidates. But *Zhu et al.* teach applying *package clock distribution design*

optimization for *high speed* and *low-power* ASICs – [title; abstract]. *Zhu et al.* also teach the following subject matter:

- Optimal design of *clock network* (i.e., *clock trees*) by taking advantages of *package layers*, which provide *1000 times less wire resistance* and *10 time less wire capacitance* than those of (nominal) *interconnects* (i.e., *conductive wiring patterns*, *metal route paths*) on (ASIC) chip – [abstract]; Notice that *high speed* and *low-power* of the *clock network* are due to *less wire resistance* and *less wire capacitance* of the package layers;
- *Transmission line noise suppression* for *package clock trees* – [abstract; Fig. 2]; *global clock tree* can be assigned on package – [Fig. 2; page 57, left col.]; Notice that (1) *global clock tree* can be *package clock tree* (2) *global clock tree* can be constructed using *transmission line* in order to suppress *noise*, (3) paths in *clock trees* are route paths for *transmission line replacement candidates*.

Notice that the *route paths* between the ASIC are *examined* (i.e., *scanned*) to determine *route paths* in *clock trees* for *transmission line replacement candidates* in order to construct *global clock trees* using *transmission line* thereby achieving high-speed and low-power performance of the ASIC.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Zhu et al.* in scanning (examining) the route paths to determine *clock trees* for *transmission line replacement candidates* in order to construct *global clock trees* using *transmission line* thereby achieving high-speed and low-power performance of the ASIC.

Zhu et al. also show in Fig. 2 and teach that, for each *transmission line replacement candidate* (i.e., a *route path* in *clock tree*), automatically selecting a *buffered wire* to implement a route path in *local **clock tree*** or a *transmission line* to implement a route path in *global **clock tree***.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

7. As to Claim 8, reasons are included in **[Response A]** given above. Notice that the explanations included in **[Response A]** could be applied in generating program codes of

program product stored on a recordable medium for routing communication lines between blocks of an ASIC as recited in Claim 8.

8. As to Claim 14, reasons are included in **[Response A]** given above. Notice that the explanations included in **[Response A]** could be applied in design of a design tool having a set of systems for routing communication lines between blocks of an ASIC as recited in Claim 14.

9. As to Claim 2, reasons are included in **[Response A]** given above, Notice that (1) there are a plurality of interconnecting wirings (route paths) between functional blocks of the ASIC, (2) each route path in the *local **clock tree*** are routed using wire with buffers, and each route path in the global ***clock tree*** are routed using transmission line without buffers – [Fig. 2].

For reference purposes, the explanations given above in response to Claim 2 are called **[Response B]** hereinafter.

10. As to Claims 9 and 15, reasons are include in **[Response B]** given above.

11. As to Claim 3, Zhu et al. show in Fig. 2 and teach in **[Response A]** that each *route path* of *global clock tree* is a *transmission line* built in package layer, which passes over a functional block of the ASIC without using a buffer.

For reference purposes, the explanations given above in response to Claim 3 are called **[Response C]** hereinafter.

12. As to Claims 10 and 16, reasons are include in **[Response C]** given above.

13. Claims 7 and 20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,702,868 to *Kellam et al.* and IEEE paper entitled "*Package Clock Distribution Design Optimization for High-Speed and Low-Power VLSIs*" to *Zhu et al.* in view of U.S. Patent Application Publication No. 2004/0090282 A1 to *Minami.*

14. As to Claim 7, Kellam et al. and Zhu et al. teach all subject matter recited in Claim 1. Zhu et al. teach using *transmission line* for *route path* of *global clock tree*, they do not

teach that the transmission line comprise a *coplanar waveguide transmission line*. But Minami teach using *coplanar waveguide (transmission line)* in a region where signal lines are *highly dense* at the *clock signal supply designation* – [Paragraph 0036, line 5 – 7]. Minami also teach that the *coplanar waveguide (transmission line)* is substantially unaffected by noise due to cross talk from wiring layers – [Paragraph 0024].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Minami* in applying *coplanar waveguide transmission line* for routing route path of global clock tree without using buffer(s) *in* a region where signal lines are highly dense at the clock signal supply designation in order to avoid congest and to substantially reduced noise due to *cross talk* from adjacent signal lines.

For reference purposes, the explanations given above in response to Claim 7 are called **[Response D]** hereinafter.

15. As to Claim 20, reasons are included in **[Response D]** given above.

Allowable Subject Matter

16. Claims 4 – 6, 11 – 13 and 17 – 19 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because the prior art does not teach or fairly suggest the following subject matter:

- A method of automatically selecting a buffered wire or a transmission line to implement the route path comprises providing a *look-up table* containing *process specific parameters* of the *transmission line* in combination of the limitations as recited in Claim 4;
- A program code for automatically selecting a buffered wire or a transmission line to implement the route path comprises program code for accessing a *look-up table* containing *process specific parameters* of the *transmission line* in combination of the limitations as recited in Claim 11;

- A design tool having system for automatically selecting a buffered wire or a transmission line to implement the route path comprises a *look-up table* containing *process specific parameters* of the *transmission line* in combination of the limitations as recited in Claim 17.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272-1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Patent Examiner
Art Unit 2825
November 4, 2004